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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/236,062	01/22/99	ZHAO	R 33850/PYI/S6

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EXAMINER	
NGUYEN, T	
ART UNIT	PAPER NUMBER
2182	07

DATE MAILED: 08/28/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/236,062	ZHAO ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-13 and 16-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-9,14-17 and 23-34* is/are rejected.

7)☐ Claim(s) *10-13 and 18-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3,4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-34 were presented in the original application dated 01/22/99. Claims 14-15 were removed from examination by the amendment received 06/18/01, in response to the restriction requirement mailed 05/15/01. Claims 1-13 and 16-34 remain pending. The restriction requirement mailed 05/15/01 is now withdrawn. To expedite prosecution, claims 14-15 are examined with the pending claims. The Attorney for Applicant, Bradley Scheer (Reg. No. 47,059) has been informed on 08/10/01 that upon receipt of this office action, claims 14-15 can be added as new claims if Applicant still wishes to retain them.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-2, 23, 30 are rejected under 35 U.S.C. 102(e) as being anticipated **by Goettsch (U.S. Pat. No. 6,112,262)**.

4. As per claims 1-2, **Goettsch** teaches a method for providing ordered data to a device [120, Fig. 1B] over a bus [135, Fig. 1B], the bus providing a communication path

for data and associated addresses, comprising:

writing items of data into sequentially ordered areas of a memory to form a sequence of items of data [7, 3, 5, Rectangle, Yes, Mix, Fig. 6], the sequentially ordered areas of memory being identifiable by addresses, each item of data being placed in an area having an associated address [Fig. 6 - item of data 7 is placed in a memory area having an address associated with a dummy address and bit 1 of the information word sent in bus cycle 1 Fig. 6];

transmitting the items of data and the associated addresses [Fig. 6 - information word in bus cycle 1 and dummy address] over the bus;

receiving the items of data and the associated addresses from the bus;

examining the associated address for each item of data received from the bus; and

placing each item of data received from the bus in one of the multiple sequentially arranged areas of a storing buffer [180, Fig. 1B], each item being placed based on the associated address of each item, the placement of the items of data forming the sequence of items (col. 5, line 54-col. 9, line 63).

Goettsch further teaches the items of data comprising commands [Bit 9, Fig. 4] and parameters [Bits 1-8, 10-13, Fig. 4], with each parameter pertaining to a command.

5. As per claim 23, Goettsch teaches a computer device for reordering incoming data received from a bus interface [132, Fig. 1B], the incoming data having associated address information [Fig. 6 - information word in bus cycle 1], comprising:

a receive buffer [140, Fig. 1B] which receives the incoming data;

a storage buffer [180, Fig. 1B] which stores the incoming data in an order based on the associated address information; and

a decoder [160, Fig. 1B] which determines proper placement of the incoming data in the receive buffer in the storage buffer based on the associated address information (col. 5, line 54-col. 9, line 63).

6. As per claim 30, Goettsch teaches a method for reordering incoming data from a data source [130, Fig. 1B], the incoming data containing address information [Fig. 20; col. 16, lines 5-25], the incoming data being in a predefined order in the data source (address1/ data1/address2/data2/...) and being transmitted from the data source in an order (dummy address1/address1/dummy address2/data1/dummy address3/address2/ dummy address4/data2/...) other than the predefined order (col. 15, line 56-col. 16, line 25), the method comprising:

receiving the incoming data transmitted from the data source [140, Fig. 1B];

arranging, in the predefined order, the incoming data based on the address information contained within the incoming data [Fig. 21; col. 16, lines 25-44]; and

storing the arranged data temporarily (col. 16, lines 25-44).

7. Claims 23-25 and 30-34 are rejected under 35 U.S.C. 102(e) as being anticipated **by Palanca et al. (U.S. Pat. No. 6,122,715)**.

8. As per claim 23, **Palanca et al.** (Palanca) teaches a computer device [100, Fig. 1] for reordering incoming data received from a bus interface [200, Fig. 2], the incoming data having associated address information [422, 416, Fig. 3], comprising:

a receive buffer [326, Fig. 2] which receives the incoming data;

a storage buffer [370, Fig. 2] which stores the incoming data in an order based on the associated address information [Figs. 3, 6-9]; and

a decoder [340, Fig. 2] which determines proper placement of the incoming data in the receive buffer in the storage buffer based on the associated address information (col. 7, lines 11-14; col. 7, lines 19-24; col. 9, lines 48-63).

9. As per claims 24-25, Palanca teaches a tag array [11 01 in Y fields of fill buffer control field 810, Fig. 7 corresponding to buffers 0, 1, 2, 3] to indicate that data is stored in a portion within the storage buffer (col. 10, lines 19-40); and hit arrays [WCM, WCB, WCE fields of fill buffer control field 810, Fig. 7] to indicate that data cannot be stored in a specific portion within the storage buffer (col. 7, lines 41-55; col. 10, lines 41-65).

10. As per claim 30, Palanca teaches a method for reordering incoming data from a data source [326, Fig. 2], the incoming data containing address information [422, 416, Fig. 3], the incoming data being in a predefined order in the data source [220, 326, Fig. 2], the method comprising:

receiving the incoming data transmitted from the data source [250, Fig. 2];

arranging, in the predefined order, the incoming data based on the address information contained within the incoming data [Figs. 6-9; col. 7, lines 11-14; col. 7, lines 19-24; col. 9, lines 48-63]; and

storing the arranged data temporarily [before eviction – S650, Fig. 5].

11. As per claims 31-34, Palanca teaches indicating that the arranged data is temporarily stored [S630, S640, Fig. 5; col. 7, lines 48-55]; storing the arranged data into a series of blocks of contiguous data [DATA field having 8 bytes, Fig. 6; col. 9, lines 58-63]; processing the arranged data stored in the predefined order [path B, Fig. 2; col. 7, lines 19-24]; and indicating that the arranged data that is temporarily stored is being processed (col. 7, lines 48-49).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 3-9, 14-15, 24-29, 31-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Goettsch**. The rejections of claims 1-2, 23, and 30 above as being anticipated by Goettsch are incorporated by reference.

14. As per claims 3-4, it would have been obvious to one of ordinary skill in the art at the time the invention was made that in order to create the information word, the items of data need to be examined to determine whether the items of data are commands or parameters, and to determine which parameters pertain to a command.

15. As per claim 5, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a storing buffer is used for storing an item of data that would be read later.

16. As per claims 6-8, Goettsch teaches the claimed invention except for an associated read availability status array comprising a plurality of read availability indicators, with each of the multiple sequentially arranged areas of the storing buffer having a corresponding read availability indicator to indicate data availability for reading when data is placed in the corresponding area of the storing buffer, and data unavailability for reading when data is read from the corresponding area of the storing buffer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include such an array in Goettsch's teachings since it was well known in the art at the time the invention was made that such an array was often associated with a storage buffer to indicate data availability/unavailability for reading in an area of the storage buffer.

17. As per claim 9, Goettsch teaches the storing buffer comprising a plurality of registers [Fig. 3]. It would have been an obvious matter of design choice to one of ordinary skill in the art at the time the invention was made to implement the storing buffer as a plurality of storage buffers, with each of the storage buffers having an associate read availability status array since it appears that the invention would perform equally well with a plurality of registers and associated read availability status array being used to implement the storing buffer.

18. As per claims 14-15, Goettsch teaches the claimed invention (see rejections to claims 1-4 above) except for the region of the memory being defined as a write combining memory type. It would have been an obvious matter of design choice to one of ordinary skill in the art at the time the invention was made to define the region of the memory as a write combining memory type, since it appears that the invention would perform equally well with any type of memory.

19. As per claims 24-25, Goettsch teaches the claimed invention except for the storage buffer comprising a tag array to indicate that data is stored in a portion within the storage buffer, and the storage buffer comprising hit arrays to indicate that data cannot be stored in a specific portion within the storage buffer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include such tag array and such hit arrays in Goettsch's teachings since it was well known in the art at the time the invention was made that such tag array was often associated with

a storage buffer to indicate that data is stored in a portion within the storage buffer, and that such hit arrays were often associated with a storage buffer to indicate that data cannot be stored in a specific portion within the storage buffer.

20. As per claim 26, Goettsch teaches the storage buffer for storing graphics commands and parameters (col. 8, lines 10-17) before forwarding them to a processing engine [170, Fig. 1B], therefore obviously teaches a graphics memory connected to the storage buffer. It was further well known in the art that graphics memory was able to store blocks of data retrieved from a storage buffer (**Glew: U. S. Pat. No. 5,561,780**).

21. As per claim 27, Goettsch teaches a central processor [110, Fig. 1B]; and inherently a computer program executing on the central processor for sending the incoming data over the bus interface.

22. As per claims 28-29, Goettsch teaches the claimed invention except for the receive buffer being a FIFO, and for the storage buffer comprising a plurality of 32 bits Dwords. It would have been an obvious matter of design choice to one of ordinary skill in the art at the time the invention was made to use a FIFO as the receive buffer and to implement the storage buffer as a plurality of 32 bits Dwords since applicant has not disclosed that those features solve any stated problem or is for any particular purpose and it appears that the invention would perform equally well with one of several types of receive buffer or a storage buffer of with a different length or number of bits.

23. As per claims 31-34, see the rejections to claims 6-8, 24-25 and 26 as being unpatentable over Goettsch above. Goettsch further teaches the arranged data being stored in the predefined order (col. 60, lines 40-44).

24. Claims 1-9, 16-17, and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Palanca**.

25. As per claim 1, Palanca teaches a method for providing ordered data to a device [135, Fig. 1] over a bus [115, Fig. 1], the bus providing a communication path for data and associated addresses, comprising:

writing items of data into sequentially ordered areas of a memory to form a sequence of items of data [740, 760, Fig. 1: DATA field comprising sequence of items of data], the sequentially ordered areas of memory being identifiable by addresses [740, 760, Fig.1: ADDRESS field and BW control field], each item of data being placed in an area having an associated address [740, 760, Fig.1: ADDRESS field and BW control field];

transmitting the items of data and the associated addresses over the bus;

receiving the items of data and the associated addresses from the bus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that Palanca's purpose of providing an ADDRESS field and a BW control field is to use the information in those two fields to place data items in the DATA

field in a destination area, and that the placement of the items would form the sequence of items with respect to fill buffer control fields 740, 760, Fig. 1. Palanca, therefore, obviously teaches examining the associated address for each item of data received from the bus; and placing each item of data received from the bus in a storing buffer, each item being placed based on the associated address of each item, the placement of the items of data forming the sequence of items.

Palanca does not specifically teach placing each item of data in one of the multiple sequentially arranged areas of a storing buffer. It is, however, well known in the art at the time the invention was made for placing data items from write combine buffers in one of the multiple sequentially arranged areas of a frame buffer before display (see **Glew, U. S. Pat. No. 5,561,780** to same assignee as Palanca's: col. 11, lines 44-57). Because applicant's invention is directed to graphics application, it would have been obvious to one of ordinary skill in the art at the time the invention was made that Palanca also teaches placing each item of data in one of the multiple sequentially arranged areas of a frame buffer, hence a storing buffer.

26. As per claims 2-4, it is well known in the art at the time the invention was made for items of data transferred on the same bus to comprise of commands and parameters, and for each parameter to pertain to a command; such features therefore being either obvious or inherent in Palanca's teachings. It would have been also obvious to one of ordinary skill in the art at the time the invention was made to examine the items of data to determine whether the items of data are commands or parameters,

and to determine which parameters pertain to a command when items of data comprising commands and parameters are transferred on the same bus.

27. As per claim 5, it would have been obvious to one of ordinary skill in the art at the time the invention was made that a storing buffer is used for storing an item of data that would be read later.

28. As per claims 6-8, Palanca teaches the claimed invention except for an associated read availability status array comprising a plurality of read availability indicators, with each of the multiple sequentially arranged areas of the storing buffer having a corresponding read availability indicator to indicate data availability for reading when data is placed in the corresponding area of the storing buffer, and data unavailability for reading when data is read from the corresponding area of the storing buffer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include such an array in Palanca's teachings since it was well known in the art at the time the invention was made that such an array was often associated with a storage buffer to indicate data availability/unavailability for reading in an area of the storage buffer.

29. As per claim 9, Palanca obviously teaches the storing buffer comprising multiple sequentially arranged areas (rejection of claim 1 in paragraph 25 above). It would have been an obvious matter of design choice to one of ordinary skill in the art at the time the

invention was made to implement each sequentially arranged area as a individual storage buffer, with each storage buffer having an associate read availability status array since it appears that the invention would perform equally well with a plurality of storage buffers and associated read availability status array being used to implement the storing buffer.

30. As per claim 16, Palanca teaches a bus interface unit [250, Fig. 2] of a computing device [100, Fig. 1], the bus interface unit coupled to a bus with a weakly ordered interface [from 326 to 250, Fig. 2] providing information comprised of data items [420, Fig. 3] and associated addresses [422, 416, Fig. 3], comprising:

a plurality of storage buffers [0, 1, 2, 3, Fig. 7], each buffer having a plurality of slots [8 slots corresponding to the bits in the BWCF, Fig. 6] for storing data items;

a router [340, Fig. 2] for routing data items received from the bus to one of the plurality of storage buffers based on the first part of the address associated with a data item [422, Fig. 3]; and

routing a data items routed to one of the storage buffers to one of the slots in that buffer based on a second part of the address associated with the data item [416, Fig. 3].

Palanca, therefore, discloses the claimed invention except specifically teaching a first router routing data items based on the first part of the address associated with a data item; and a plurality of second routers, each second router routing data items within each of the storage buffers based on the second part of the address associated with the data item.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the second router function separately from the first router function, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlichman*, 168 USPQ 177, 179.

31. As per claim 17, it is well known in the art at the time the invention was made for items of data transferred on the same bus to comprise of commands and parameters, such feature therefore being either obvious or inherent in Palanca's teachings. It would have been also obvious to one of ordinary skill in the art at the time the invention was made that since commands and parameters are transferred together and stored in the plurality of slots in Palanca's teachings, a command interpreter is required for differentiating commands from parameters; hence a means for providing data items stored in the plurality of slots to a command interpreter for determining if any of the data items corresponds to a command.

32. As per claims 25-29, the rejections of claims 23-25 above as being anticipated by Palanca are incorporated by reference.

33. As per claim 25, it would also have been obvious to one of ordinary skill in the art at the time the invention was made to include hit arrays in Palanca's teachings since it was well known in the art at the time the invention was made that hit arrays were often

associated with a storage buffer to indicate that data cannot be stored in a specific portion within the storage buffer.

34. As per claim 26, Palanca teaches write combining buffers. It would have been obvious to one of ordinary skill in the art at the time the invention was made that Palanca teaches a graphics memory connected to the storage buffer and able to store blocks of data retrieved from the storage buffer since it was well known in the art at the time the invention was made for write combining buffers to store blocks of graphics data for transmission to a graphics memory (see **Glew, U. S. Pat. No. 5,561,780** to same assignee as Palanca's: frame buffer 22, Fig. 1).

35. As per claim 27, Palanca teaches a central processor [110, Fig. 1]; and inherently a computer program executing on the central processor for sending the incoming data over the bus interface.

36. As per claims 28-29, Palanca teaches the claimed invention except for the receive buffer being a FIFO, and for the storage buffer comprising a plurality of 32 bits Dwords. It would have been an obvious matter of design choice to one of ordinary skill in the art at the time the invention was made to use a FIFO as the receive buffer and to implement the storage buffer as a plurality of 32 bits Dwords since applicant has not disclosed that those features solve any stated problem or is for any particular purpose

and it appears that the invention would perform equally well with one of several types of receive buffer or a storage buffer of with a different length or number of bits.

Allowable Subject Matter

37. Claims 10-13, 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

38. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cheriton (U. S. Pat. No. 5,893,155) teaches a log block builder combining write operations into data blocks and transfers the data blocks to a log splitter, which demultiplexes the logged data into separate streams based on address.

Glew et al. (U. S. Pat. No. 5,561,780) teaches graphics write operations within an out-of-order microprocessor being combined into cache-line-size buffers, then transmitted to a frame buffer using a burst mode eviction.

39. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Quang Nguyen whose telephone number is (703) 305-0138, and whose e-mail address is tanh.nguyen36@uspto.gov. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee, can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 306-5404.

Any inquiry of a general nature relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Mail responses to this action should be sent to:

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Faxes for formal communications intended for entry should be sent to:

(703) 308-9051,

or, for informal or draft communications, to:

(703) 306-5404 (please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to:

Crystal Park II, 2121 Crystal Drive, Arlington, Va, Sixth Floor (Receptionist).

THOMAS LEE
SUPERVISORY PATENT EXAMINER
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TQN
8/26/01